Listing of the Claims

1. (Currently Amended) A memory system for data access and storage comprising:

at least first and second arrays of memory cells, wherein the first and second arrays having dissimilar operating characteristics such that one of the arrays operates faster than the other of the arrays during a read or write operation, ~~a first array characterized by a first set of properties; and a second array characterized by a second set of properties, wherein the second set of properties differs from the first set of properties, and~~

wherein the first array stores a first data packet and the second array stores a second data packet, and wherein the first and second arrays utilize a common addressing scheme and operate ~~at different speeds and~~ in conjunction with one another when reading data from said first and second arrays or writing data to said first and second arrays ~~output data~~.

2. (Canceled)

3. (Currently Amended) The memory system of claim 1 ~~2~~, and further comprising a memory controller connected to the first array and to the second array, wherein the first array operates at a first supply voltage and the second array operates at a second supply voltage, wherein the second supply voltage is less ~~higher~~ than the first supply voltage so that the first array performs read and write operations faster than said second array, and wherein a length of the signal path from the second array to a memory controller is less ~~greater~~ than a length of the signal path from the first array to the memory controller, such that, after a request for data, ~~which comprises a first data packet residing in the first array and a second data packet residing in the second array, is received by the first array and the second array,~~ an output of the first data packet of a data word ~~packet~~ from the first array and an output of the second packet of said data ~~packet~~ word ~~output~~ from the second array arrive at the memory controller at about the same time.

4. (Canceled)

5. (Currently Amended) The memory system of claim 1 [[4]], and further comprising a memory controller connected to the first array and to the second array, wherein the first array

comprises a wordline length that is shorter than a wordline length of the second array ~~comprises a second wordline length wherein the wordline length of the second array is greater than wordline length of the first array~~, and wherein a length of the signal path from the second array to a memory controller is less than a length of the signal path from the first array to the memory controller, such that, after a request for data, ~~which comprises a first data packet residing in the first array and a second data packet residing in the second array, is received by the first array and the second array,~~ an output of the first data packet of a data word from the first array and an output of the second data packet of said data word ~~output~~ from the second array arrive at the memory controller at about the same time.

6. (Currently Amended) The memory system of claim 5, wherein the first array is connected to an operating voltage that is different than an operating voltage connected to the second array ~~second array uses a higher supply voltage than the supply voltage used by the first array, such that, after a request for data, which comprises a first data packet residing in the first array and a second data packet residing in the second array, is received by the first array and the second array, an output of the first data packet from the first array and an output of the second data packet output from the second array arrive at the controller at about the same time~~.

7. (Currently Amended) The memory system of claim 1, wherein the first array comprises ~~bitline~~ sensing circuitry ~~set at~~ connected to and driven by a system supply voltage, and the second array comprises ~~bitline~~ sensing circuitry connected to and driven by a ~~operating at~~ ground potential such that the first array has a faster cycle time than the second array but the first array has a longer latency interval than the second array.

8. (Currently Amended) A method for storing data in and retrieving data from a semiconductor memory, comprising:

~~linking a memory controller to~~ storing a first data packet in a first memory array having ~~characterized by~~ a first set of operating characteristics ~~properties~~;

~~linking the memory controller to~~ storing a second data packet in at least one other memory array having ~~characterized by~~ a second set of operating characteristics that are different from the first set of operating characteristics such that the one of the memory arrays operates

faster than the other of the memory arrays but data is stored in the first memory array and the at least one other memory array using a common addressing scheme ~~properties, wherein the first and second set of properties are different~~; and

~~storing a data packet, wherein a portion of the data packet is stored in the first array, and the remaining portion of the data packet is stored in the at least one other array; and~~

retrieving the first and second data packets from the first memory and the at least one other memory array to account for the different operating characteristics of the first memory array and the at least one other memory array ~~packet, wherein the data packet is retrieved in at least two portions by, a first portion residing in the first array characterized by a first set of properties, and the remaining portion residing in the at least one other array characterized by a second set of properties~~.

9. (Currently Amended) The method of claim 8, and further comprising simultaneously signaling the first memory array and the at least one other memory array to perform a read operation, wherein said retrieving is performed after said ~~the data packet is retrieved after~~ simultaneously signaling such that the first portion of the data packet is output from the first memory array slightly before the second portion of the data is output from the at least one other memory array ~~the first array and the at least one other array to output the data packet~~.

10-12. (Canceled)

13. (Currently Amended) The method of claim 8 ~~12~~, wherein said retrieving is performed to account for ~~the~~ a latency of the first memory array being ~~is~~ less than ~~the~~ a latency of the second memory array and a ~~the~~ cycle time of the first memory array being ~~is~~ greater than a ~~the~~ cycle time of the at least one other memory array.

14. (Currently Amended) The method of claim 13, wherein said retrieving comprises retrieving a multiple byte information packet by retrieving a byte from the first memory array followed by retrieving a byte from the second array ~~the data packet is output in a plurality of sub-portions, the output sequence of the sub-portions being arranged in an ordered series, wherein the first array outputs the first sub-portion, and the second array outputs the second sub-portion~~.

15. (Currently Amended) A memory device, comprising:

a first memory array;

a second memory array having operating characteristics dissimilar to operating characteristics of the first memory array but using the same addressing scheme that is used by the first memory array such that one of the arrays operates faster than the other of the arrays during a read or write operation;

a memory controller;

a memory bus connected to said ~~in communication with a~~ memory controller~~, wherein the first and second memory arrays utilize a same addressing scheme, wherein the first and second memory arrays have at least one property different from one another,~~ and wherein for a given data retrieval event in the memory device, the first memory array outputs a first portion of data consistent with the data retrieval event and the second memory array outputs a second portion of data consistent with the data retrieval event, wherein the first portion of data and the second portion of data are received at the memory controller at about the same time.

16-20. (Canceled)

21. (New) The memory system of claim 7, and further comprising a memory controller connected to the first array and to the second array, wherein the first data packet stored in the first array is a byte and the second data packet stored in the second array corresponds to is a byte, and wherein the memory controller reads a multi-byte information packet from the first and second arrays by reading a first byte from the second array followed by reading a second byte from the first array followed by reading a third byte from the second array.

22. (New) The memory system of claim 1, wherein the first array has a refresh rate and refresh current that is greater than a refresh rate and refresh current for the second array.

23. (New) The memory system of claim 1, wherein the first array comprises more cells per bitline than the number of cells per bitline of the second array.

24. (New) The memory system of claim 23, wherein the second array comprises at least two sub-arrays each having the same number of cells per bitline.

25. (New) The memory device of claim 15, wherein the first memory array operates at a first supply voltage and the second memory array operates at a second supply voltage, wherein the second supply voltage is less than the first supply voltage so that the first memory array performs read and write operations faster than said second memory array, and wherein a length of the signal path from the second memory array to a memory controller is less than a length of the signal path from the first memory array to the memory controller, such that, in response to a request for data, an output of the first portion from the first memory array and an output of the second portion from the second memory array arrive at the memory controller at about the same time.

26. (New) The memory device of claim 15, wherein the first memory array comprises a wordline length that is shorter than a wordline length of the second memory array, and wherein a length of the signal path from the second memory array to a memory controller is less than a length of the signal path from the first memory array to the memory controller, such that, in response to a request for data, an output of the first portion from the first memory array and an output of the second data portion from the second memory array arrive at the memory controller at about the same time.

27. (New) The memory device of claim 15, wherein the first array comprises sensing circuitry connected to and driven by a system supply voltage, and the second array comprises sensing circuitry connected to and driven by a ground potential such that the first array has a faster cycle time than the second array but the first array has a longer latency interval than the second array.

28. (New) The memory device of claim 27, wherein the first portion stored in the first array is a byte and the second data packet stored in the second array corresponds to is a byte, and wherein the memory controller reads a multi-byte information packet from the first and second

arrays by reading a first byte from the second array followed by reading a second byte from the first array followed by reading a third byte from the second array.

29. (New) The memory device of claim 15, wherein the first array has a refresh rate and refresh current that is greater than a refresh rate and refresh current for the second array.

30. (New) The memory device of claim 15, wherein the first array comprises more cells per bitline than the number of cells per bitline of the second array.

31. (New) The memory device of claim 30, wherein the second array comprises at least two sub-arrays each having the same number of cells per bitline.